Padmanabhan, Mano

From: Namazi, Mehdi
Sent: Wednesday, December 22, 2004 4:14 PM
To: Padmanabhan, Mano
Subject: FW: 09/857022

-----Original Message-----
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Exr. Namazi–

Here are the proposed claim amendments.

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Proposed Claims

14. (Previously Presented) An interleave address generation apparatus of a block interleave system, generating a read address or a write address of data arranged in the form of a matrix two dimensional array, said interleave address generation apparatus comprising:

a counter that outputs a row number and a column number on the two dimensional array in the block interleave system;

a bit inversion section that inverts a bit of the row number;

a column exchange section that outputs an address value corresponding to the bit inverted row number and the column number as a column conversion value;

a shift register that shifts the bit of the bit inverted row number and outputs the shifted bit as an address offset value;

an adder that adds the address offset value and the column conversion value; and

a size comparison section that compares the addition value to an interleave size and outputs the addition value within the interleave size as an address value.

15. (Previously Presented) The interleave address generation apparatus according to claim 14, wherein said bit inversion section switches a higher bit and a lower bit based on the row number output from said counter.

16. (Previously Presented) The interleave address generation apparatus according to claim 14, further comprising a storage cell array that stores the bit inverted row number on a temporary basis and thereafter outputs said row number to said shift register.

17. (Previously Presented) The interleave address generation apparatus according to one of claims 14 to 16, wherein said interleave address generation apparatus is used in a Galois field interleave system.

18. (Previously Presented) The interleave address generation apparatus according to one of claims 14 to 16, wherein said column exchange section comprises:

first storing means that stores a first unique constant value on a per row basis based on the bit inverted row number;

second storing means that stores a second unique constant value on a per column basis;

an exclusive logical sum calculator that performs an exclusive logical sum calculation of the stored first and second unique constant values; and

third storing means that stores the exclusive logical sum calculation value as the address value.

19. (Previously Presented) A turbo coding apparatus comprising a recursive convolutional coder that performs a convolutional coding of an information series and an interleaver that comprises the interleave address generation apparatus of one of claims 14 to 16.

20. (Previously Presented) A turbo decoding apparatus comprising:

a first soft decision output decoder that decodes a code series;

an interleaver that comprises the interleave address generation apparatus of one of claims 14 to 16 that performs interleave processing of an output from said first soft decision output decoder;

a second soft decision output decoder that decodes the code series in which a sequence of input data has been changed by said interleaver; and

a deinterleaver that comprises the interleave address generation apparatus of one of claims 14 to 16 that performs deinterleave processing of an output from said second soft decision output decoder.

21. (Currently Amended) A communication terminal apparatus comprising:

a decoding processing apparatus having ~~the~~ a turbo decoding apparatus ~~of claim 20~~ that comprises a first soft decision output decoder that decodes a code series, an interleaver that comprises the interleave address generation apparatus of one of claims 14 to 16 that performs interleave processing of an output from said first soft decision output decoder, a second soft decision output decoder that decodes the code series in which a sequence of input data has been changed by said interleaver, and a deinterleaver that comprises the interleave address generation apparatus of one of claims 14 to 16 that performs deinterleave processing of an output from said second soft decision output decoder, wherein said turbo decoding apparatus decodes a demodulated received signal; and

a coding processing apparatus having ~~the~~ a turbo coding apparatus ~~of claim 19~~ that comprises a recursive convolutional coder that performs a convolutional coding of an information series and an interleaver that comprises the interleave address generation apparatus of one of claims 14 to 16, wherein said turbo coding apparatus codes a transmission signal.

22. (Currently Amended) A base station apparatus comprising:

a decoding processing apparatus having ~~the~~ a turbo decoding apparatus ~~of claim 20~~ that comprises a first soft decision output decoder that decodes a code series, an interleaver that comprises the interleave address generation

apparatus of one of claims 14 to 16 that performs interleave processing of an output from said first soft decision output decoder, a second soft decision output decoder that decodes the code series in which a sequence of input data has been changed by said interleaver, and a deinterleaver that comprises the interleave address generation apparatus of one of claims 14 to 16 that performs deinterleave processing of an output from said second soft decision output decoder, wherein said turbo decoding apparatus decodes a demodulated received signal; and

a coding processing apparatus having ~~the~~ a turbo coding apparatus ~~of claim 19~~ that comprises a recursive convolutional coder that performs a convolutional coding of an information series and an interleaver that comprises the interleave address generation apparatus of one of claims 14 to 16, wherein said turbo coding apparatus codes a transmission signal.

23. (Previously Presented) An interleave address generation method of a block interleave system, generating a read address or a write address of data arranged in the form of a two dimensional matrix, said interleave address generation method comprising:

counting up and outputting a row number and a column number on a two dimensional array in the block interleave system;

inverting the row number;

determining an address value corresponding to the bit inverted row number and the column number as a column conversion value;

determining an address offset value by shifting a bit of the bit inverted row number;

adding the address offset value and the column conversion value;

comparing the addition value to an interleave size; and

outputting the addition value within the interleave size as an address value.